





TURTLE Four Weddings and a Tutorial

L. Apvrille, P. de Saqui-Sannes

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Rationale

- Verification-centric modeling of real-time and distributed systems
 - Real-time UML profile grounded in formal methods
 - Press-button approach hiding the inner workings of verification tools

• TURTLE (Timed UML and RT-LOTOS Environment)

- Formal semantics
 - Translation to RT-LOTOS and UPPAAL
- Tool: TURTLE Toolkit (TTool)
 - Alcatel-Lucent, Texas Instruments, Freescale, DoceaPower, FP7
 EVITA project (BMW, Bosch, ..), FP7 SACRA Project (Infineon, ...)
- Method
- Need for tutorials and educational case studies !



TURTLE : a Formal UML profile supported by TTool

Requirement capture

SysML Requirement Diagrams, chronograms (UML Timing Diagrams)

Automatic synthesis of observers

Use-case driven analysis, scenarios **Rendezvous and FIFO, Time intervals**

Formal verification (RTL, CADP, UPPAAL) Automatic synthesis of design diagrams

Object-oriented design Architecture, Behaviors **Object composition (process algebra) Synchronization actions, Time intervals**

Formal verification (RTL, CADP, UPPAAL)

Rapid prototyping Components, Deployment nodes Java annotations

Formal verification (RTL, CADP, UPPAAL) Java and SystemC code generators

Method and Diagrams



Future Air Navigation System



Requirement Capture

• The IN procedure either completes within 10 minutes or aborts. The pilot accordingly receives a "success" or "abortion" report.



Analysis

- A Use-Case Diagram without boot, power-off, and maintenance
- An Interaction Overview Diagram (IOD) structures elementary scenarios expressed by sequence diagrams
 - Initial Notification (connection set up, connection not established)
- Formal verification based on reachability analysis
 - Initial Notification
 - Req 1 and IN_Abortion_Report
 - Minimization
 - IN_Time_Constraint
 - Dynamic Timed Automaton
 - (observer)

Analysis: Use Case Diagram of RFN



Analysis: IOD RFN



Analysis: SD « RFN_NoLoss »



Design

- Automatic generation of design diagrams
 - From the Interaction Overview and Sequence diagrams

Hand-made enhancements

- Class/Object diagram (on next slide!)
 - Parameterized messages with complex data structures
- Activity diagrams
 - Routing inside the communication medium

• Formal verification

- Graph minimization and model-checking
- Observers



Design: Excerpt of the Activity Diagram of the class « ATCEmbeddedSystem »



Design: Formal Verification



	Verify with UPPAAL: options			
	Search for absence of deadock situations			
	✓ Reachability of selected states			
	✓ Liveness of selected states			
	Custom verification			
	Custom formulae = A<> Req2_Ob;			
	Generate simulation trace			
	Show verification details			
RFN_Begin RFN_Done maxRFNDelay	Senuing OPPAAL Specification uata			
	Reachability of: Action state (RFN_Begin) -> property is satisfied			
	Reachability of: Action state (error) -> property is NOT satisfied			
	Reachability of: Action state (error) -> property is NOT satisfied			
	Reachability of: Action state (IN_Done) -> property is satisfied			
	Liveness of: Action state (RFN_Begin) -> property is NOT satisfied			
	Liveness of: Action state (error) -> property is NOT satisfied			
	Liveness of: Action state (error) -> property is NOT satisfied			
	Liveness of: Action state (IN_Done) -> property is satisfied			
	Studying custom CTL formulae -> property is satisfied			
Model-checking	All Done			
would checking				

Prototyping

- Mapping « software components » on execution nodes
- Generating prototype code
- Deployment diagram
 - Embedded system of the aircraft
 - Air Control Tower #1
 - Air Control Tower #2
 - Communication system (Routing application)
- Automatically generated Java code
- Execution Trace

Prototyping: Deployment Diagram



Prototyping: Execution Trace

Aircraft (neac)	Router (orgnac)	ATC1 (regirock)
Aircraft (neac) Neac] java MainClass_neac_PkgAircraft Sending !i4!i0!i0!iltoorgnac/172.18.20.25 Waiting for a packet 	Router (orgnac) [orgnac] java MainClass_orgnac_PkgRouter Waiting for a packet Got packet: !4!0!0!1 Sending !i4!i0!i0!i1toregirock/172.18.20.20 Waiting for a packet	ATC1 (regirock) [regirock] java MainClass_regirock_PkgATC1 Waiting for a packet Got packet: !4!0!0!1 Sending !15!10!11!10toorgnac/172.18.20.25
a a status a seconda a seconda A seconda a seconda a A seconda a		Sending !il!i0!il!i0toorgnac/172.18.20.25 Waiting for a packet
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Conclusions

• Contributions

- A verification-centric UML profile
- A method for real-time and distributed system design
- TURTLE toolkit (TTool)
 - http://labsoc.comelec.enst.fr/turtle/ttool.html

• Projects that used TURTLE and TTool (selection)

- SAFECAST (secured group communication system)
- EVITA (modeling and proof of security properties in vehicle embedded systems)
- DoceaPower (modeling of power managers)

Ongoing work

- Extended Requirement Diagrams with security requirements
- Dimensioning diagrams (Network Calculus)
- DIPLODOCUS (Modeling and simulation of Systems-on-chip)